FPGA Implementations of Low Latency Centroiding Algorithms for Adaptive Optics

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Abstract: We describe two innovative low latency centroiding algorithms implemented in an FPGA, exploiting the parallel processing features of these devices, and showing low values in latency and real estate, which eases their integration with complete adaptive optics systems.

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1. Introduction

The accurate detection of centroids in a wavefront sensor has a strong impact in the overall performance of an Adaptive Optics (AO) system. Center of Gravity (CoG) algorithm and its variations are commonly used to detect centroid coordinates in the image sensor plane. Some researchers have implemented complete AO systems in different computing devices [1], but not too much work has been accomplished using Field Programmable Gate Array (FPGA) devices [2].

FPGA are digital reconfigurable computing devices, consisting in massive arrays of logic gates and complex processing units such as multipliers or logic memories. They are well suited for processing parallel data streams in real time in a pipelined fashion, therefore they work well processing data coming from CCD or CMOS image sensors.

We have designed and implemented image processing algorithms in FPGA for several applications, like adaptive optics for Astronomy and Space Situational Awareness (SSA) [3]; in particular the First Fourier Coefficient (1FC) and the Stream-based Center of Gravity (SCoG) algorithms. We have added timing performance tests to 1FC algorithm presented previously [4], and included a comparison with SCoG algorithm.

2. Description of centroiding algorithms

Fig. 1 shows the block architecture of 1FC and SCoG algorithm whose computation floats over the image, computing a result for every arriving pixel. The 1st coefficient of a Fourier series from discrete data points can be used to estimate the amount of asymmetry. Applying the shifting theorem of Fourier transform and considering only the 1st coefficient of a Fourier series, we can obtain the expression for the centroid location in X axis of the bidimensional image of 2N discrete points as:

$$\Delta x = \frac{N}{2\pi} arctan \frac{b_1}{a_1} + C_x \tag{1}$$

where C_x is the phase correction term and a_1 and b_1 are the real and imaginary part respectively. In Fig. 1(top), two counters (C_c, C_r) are the indexes of four ROM memories ($N/2\pi$ term), whose output is multiplied with stream pixel intensities $D_{IN}[9:0]$ as they are read from the sensor. The result is accumulated for each subaperture, multiplexed in M_c and M_d, and a CORDIC algorithm is used to calculate arctangent. Finally a comparator ($COMP_x$) is used to represent term C_x.

The SCoG algorithm is very similar to the traditional CoG method except that a floating CoG window is applied to each incoming pixel with its surrounding pixels. As the incoming pixels approach the true centroid of a spot, the resultant CoG value approaches zero as well due to the match of the symmetrical filter and the spot intensity distribution. In contrast to the conventional CoG method, the floating CoG window can be selected to match the spot size (3×3 shown in Fig. 1) without cutting off useful signal pixels. This SCoG operation effectively creates a local coordinate for calculating the CoG and will center on the closest pixel to the true centroid as the floating CoG window crosses by the true location of the centroid, indicating the $\mathrm{Cent_x}$ and $\mathrm{Cent_y}$ signals at that pixel. Error variance due to noisy pixels, cutting of signals by CoG window boundary and systematic bias towards the center of conventional CoG

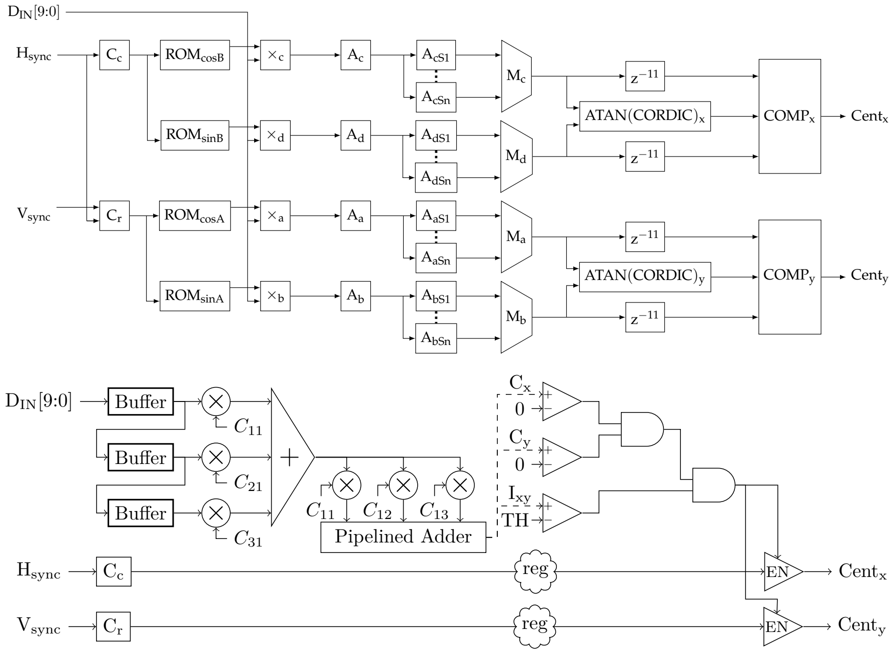

Fig. 1: 1FC (top) and SCoG (bottom) algorithm block diagrams.

window are avoided because of the flowing nature of the floating CoG window that is able to be sized to match the spot size [5].

3. Results and Conclusions

We have developed and implemented two low latency centroiding algorithms in a FPGA both suitable to be included in the processing stage of an AO system, as far as the authors are aware, not implemented before in these kind of devices. Both algorithms show latency below 2 μs.In the case of the 1FC algorithm, the FPGA utilization is around 40% for a Xilinx XC3400ADSP FPGA.

With a CMOS image sensor with rolling shutter, the system only introduced a delay of one image sensor row (6.5 μs in the case of 325 pixels per row synchronized with a 50 MHz clock) plus only 2 μs due to centroiding processing, which in most cases, is much faster than current commercial solutions [6]. This low latency allows the control system to begin determining the corrector solution almost immediately after exposing the row of the wavefront sensor and before the frame is complete.

We will show a comparison of both centroiding algorithms behavior under on-sky tests already performed with astronomical sources. It is expected to integrate these algorithms forming part of a full AO system implemented in a System On Chip (SOC) device.

References

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